TCAD Investigation of Thermal Disturb During RESET Operation in 28 nm ePCM Technology Node

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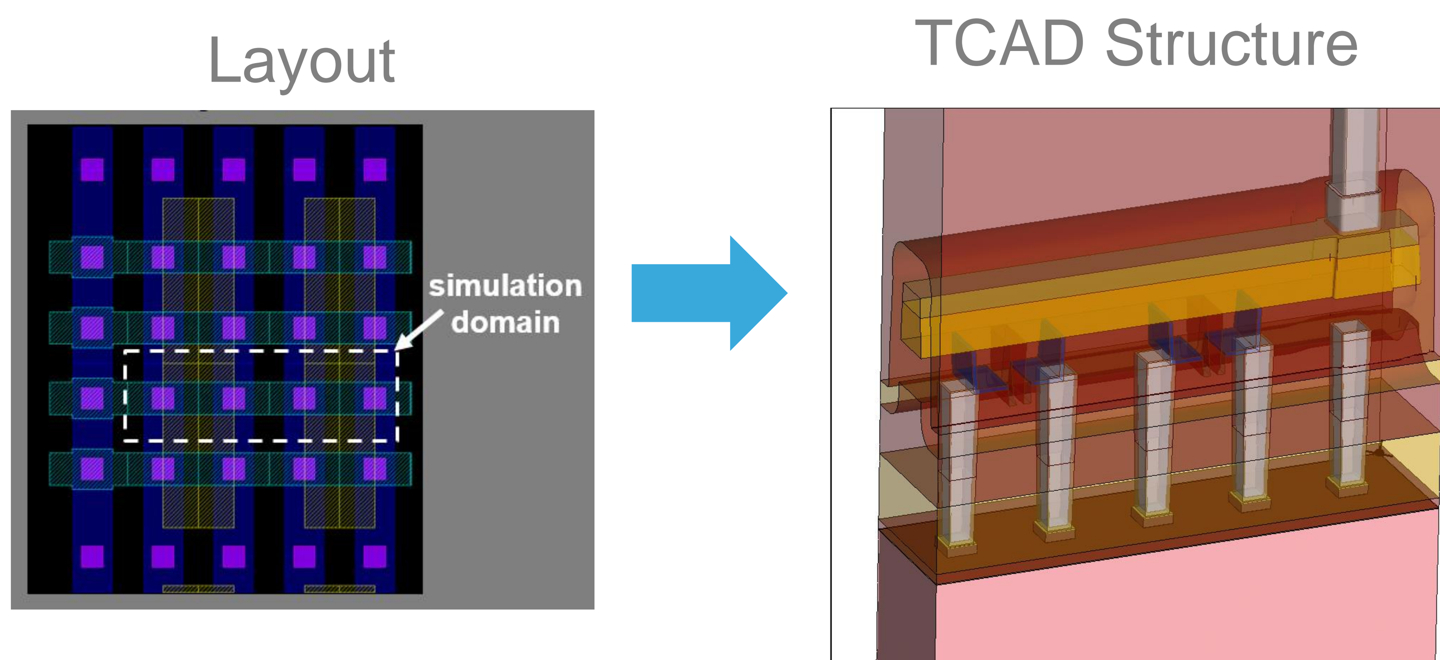
PCM Cell Architecture

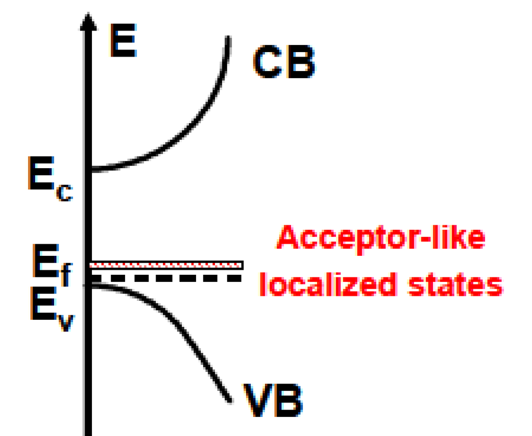


- Structure obtained from 2D layout
- TCAD Simulation tool : Sentaurus [1]
- Morphology check : TEM

[1] Sentaurus, version O-2018.06, SYNOPSYS
[2] Pirovano et al, IEEE Trans. Electron. Devices, vol. 51, no. 3, pp. 452-459, 2004
[3] Lee et al., J. Appl. Phys., vol. 97, 93509, (2005)
[4] Battaglia et al, J. Appl. Phys., vol. 107, 93509, (2010)
[5] Lyeo et al, Appl. Phys. Lett. 89, 151904 (2006)
[6] Kuwhara et al, 1st Int Symp on Thermal Design, Tsukuba, 2008
[7] Kalb, PhD Thesis, Aachen, 2002

Simulation Framework

- **GST Model** (Pirovano) [2]
  - p-type semiconductor
  - Optical bandgap : Eg = 0.5 eV [3]



- **Electrical Transport Model**
  - Drift-diffusion
  - GST mobillity

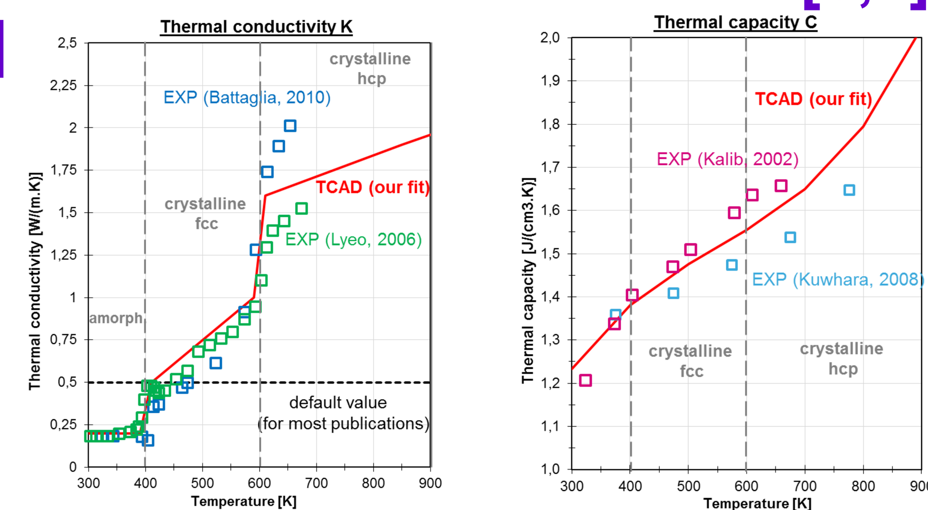
$$\vec{j}_p = -ep\mu_p(\vec{\nabla}\Phi_p + P_p\vec{\nabla}T)$$

- **Thermal Transport Model**

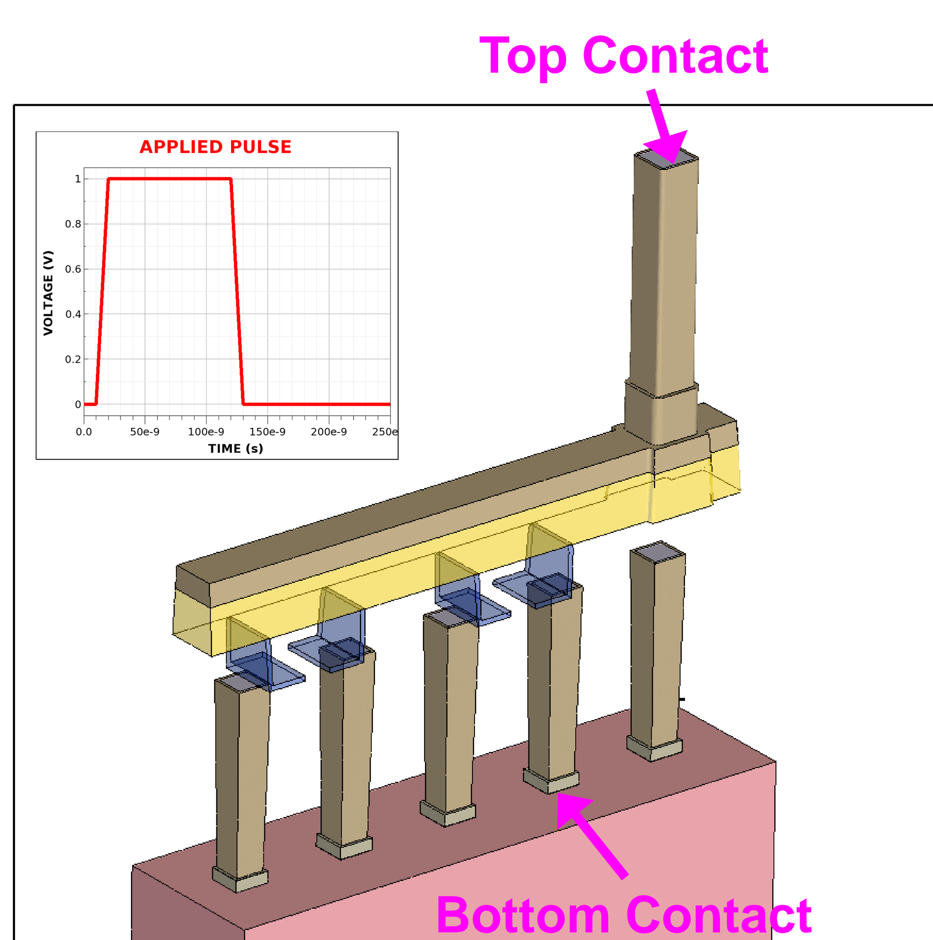
$$c_{tot}\frac{\partial T}{\partial t} = \vec{\nabla}\cdot(k_{tot}\vec{\nabla}T) + H$$

[6,7]

  - Fourier law [4,5]
  - bdry conditions
  - Material properties

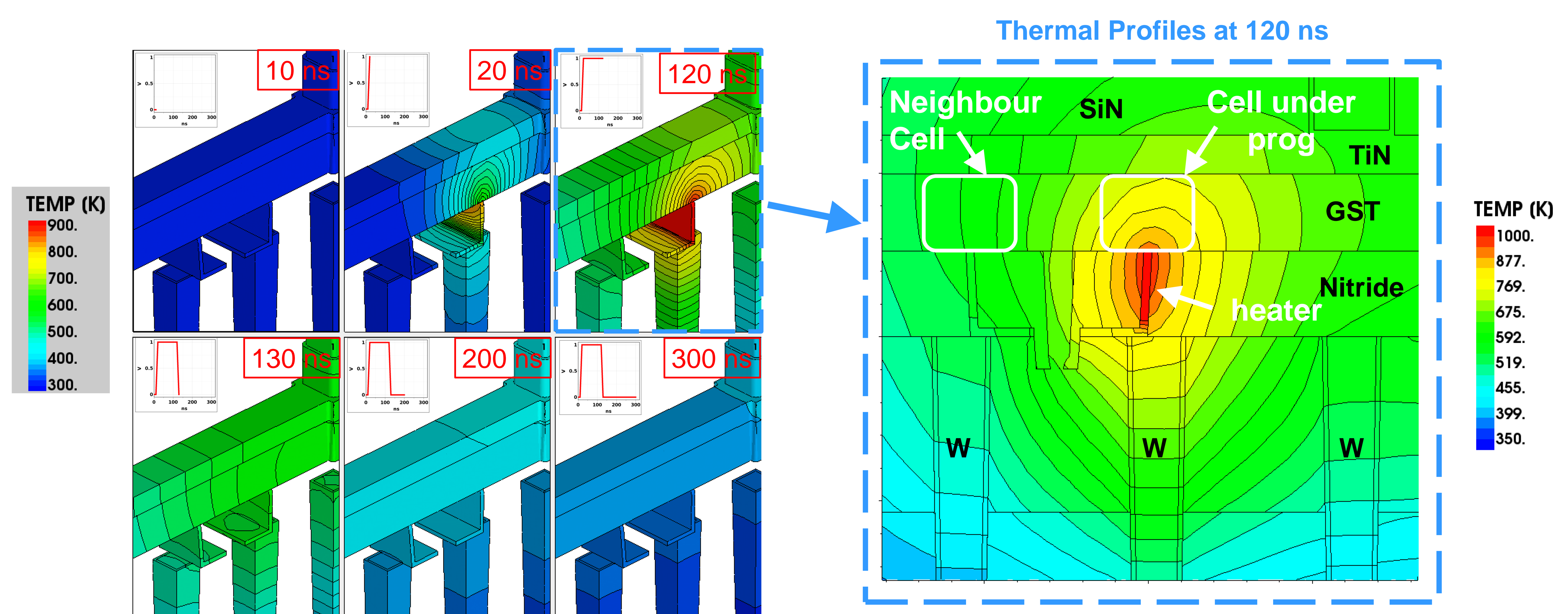


Simulation Setup



- Top contact : pulse (100 ns)
- Bottom contact : at 0 V
- Si bulk : at 300 K (heat sink)

Electro-Thermal Simulation Results



- Hot spot located at heater
- ~200 ns to reach T_{amb}
- Prog Cell : 800 K < T < 920 K
- Next Cell : 560 K < T < 630 K

Conclusion & Future work

- **Hot spot located at heater**
- **During RESET, neighbour cell T > Tcrystall (GST-225)**
- **Next : thermal disturb btw bitlines**

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